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MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
VIDWAN, JASJIT S	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/679,623
Filing Date: October 06, 2003
Appellant(s): ROLLIG ET AL.

Erik A. Heter
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/01/09 appealing from the Office action mailed 03/05/09

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

7,149,927	Stancil	12-2006
6,505,267	Luke et al	1-2003
5,581,719	Steely, Jr. et al	12-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 6-10, 15-19, 28-31 & 96 rejected under 35 U.S.C. 103(a) as being unpatentable over Stancil, U.S. Patent No: 7,149,927 **[hereinafter Stancil]** and further in view of Luke et al, U.S. Patent No: 6,505,267 **[hereinafter Luke]** and Steely, Jr. et al, U.S. Patent No: 5,581,719 **[hereinafter Steely]**.

3.

4. **As per Claim 1, 10 & 19**, Stancil teaches an SMBus host controller **[Fig. 1, element 130]** comprising:

   a. SMBus interface **[see Fig. 1, element 111]**

   b. SMBus message handler **[Fig. 1, element 110]** including finite-state machine **[Fig. 2, elements 112 & 116]** configured to manage data transfer between the SMBus interface and integrated electronic device **[Col. 4, Lines 20-32]**.

5. Stancil further teaches a system wherein the said integrated electronic device's function is not significant and thus can perform any functional logic **[see Col. 2, Line 66 – Col. 3, Line 2]**. Keeping the scope of Stancil in mind, it is submitted that Stancil does not explicitly teach a memory storing microcode, an interface to a register and further an instruction fetch unit configured to read instructions at an address from said memory. Luke teaches the above deficiency in addressing the above deficiency by disclosing a system that teaches:

(c) Memory **[See Fig. 2, element 32, 36 & 40]** configured to store microcode comprising at least two programs **[see Col. 7, Lines 58 – Col. 9, Line 12 – plurality of programs include 'Register read-modify-write', 'Register read-compare-until-match', 'Register Write', 'Register read extract nibble', 'Wait for bulk_in byte', Wait for bulk_out byte', 'DATI Push register into bulk_in', 'DATO Push bulk_out byte', 'EPPI Read EPP data register']** each for handling a bus command protocol and comprising at least one instruction **[see Col. 2, Lines 7-10 - - Also see Col. 4, Lines 66- Col. 5, Line 2]**.

(d) Interface **[Col. 4, Lines 17-21]** to a register **[see Fig. 3, element 66]** configured to identify a starting address of a program in said memory **[Col. 4, Lines 34-37]**

(e) Instruction fetch unit **[see Fig. 6, Element 90 – also see Col. 7, Lines 17-19]** configured to read an instruction at an address in said memory **[Col. 9, Lines 14-20]**, said address being specified by a program counter **[see Fig. 6, element 84]**

6. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above two teachings in order to take advantage of using memory in conjunction with Stancil's SMBus Packet Decoder/Encoder **[see Fig. 2, element 114]** to support bus protocol conversion from host to the peripheral. It is for this reason that one of ordinary skill in the art would have been motivated to combine the above two teachings.

7. Stancil and Luke teach the above limitations, however fail to teach an address register array comprising a plurality of starting addresses of programs stored in said memory. Steely teaches the above limitation of address register array comprising a plurality of starting addresses of programs stored in memory **[see Col. 3, Lines 22-45].**

8. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above teachings in order to take advantage of retrieving instructions efficiently without devoting extensive resources to determine the starting addresses of programs **[see Col. 3, Lines 8-20]**. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the above teachings.

9. **As per Claims 6, 15 and 28,** Luke and Stancil as modified above teach SMBus message handler further comprising a loop counter **[see Luke, Fig. 6, element 88]** for storing the value of a block counter register in said loop counter if the finite-state machine executed a transmit data from block counter register instruction **[see Luke, Col. 9, Lines 5-7, "DATO Push bulk_out byte into register"]**; said loop counter being decremented each time a data byte is transmitted to said SMBus interface while a "transmit data from" instruction is executed and the "transmit data from" instruction be completed when the value of said loop counter reaches zero **[see Luke, Col. 7, Lines 43-51]**.

10. **As per Claims 7, 16 and 29,** Luke and Stancil as modified above teach SMBus message handler further comprising a loop counter **[see Luke, 88]** and a block counter register **[see Luke, 66]** both for storing a byte received from said SMBus interface if the finite-state machine **[see Luke, 82]** executed a "receive data to block counter register" instruction **[see Luke, Col. 9, Lines 8-11],** said loop counter **[see Luke, 204]** being decremented each time a data byte is transmitted to or received from said SMBus interface while a "received data to block counter register " instruction is executed and the "received data to" instruction being completed when the value of said loop counter reaches zero.

11. **As per Claims 8, 17 and 30,** Luke and Stancil as modified above teach SMBus message handler, wherein each instruction comprises one bit indicating as to whether or not an instruction is the last instruction in the program **[see Luke, Col. 5, Lines 2-7]**.

12. **As per Claims 9, 18 and 31,** Luke and Stancil as modified above teach SMBus message handler, wherein each instruction comprises one bit indicating as to whether an instruction is to be executed only once or this instruction is to be executed repeatedly until a loop counter becomes zero, wherein said loop counter is decremented each time an instruction is executed repeatedly **[see Luke, Col. 7, Lines 38-57].**

13. As per Claim 96, Luke and Stancil as modified above teach a controller wherein the memory storing the microcode is a read-only memory **[see Luke, Fig. 2, element 36]**

14. Claims 2, 4, 5, 11, 13, 14, 20, 22-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Stancil and Luke and further in view of Applicant Admitted Prior Art (Description of prior art) herein after **[AAPA]**.

15. **As per Claims 2, 11 and 20**, Stancil and Luke teach the above limitations of claims 1, 10 and 19. However, Luke fails to teach a system wherein the register set complies with the ACPI specification. AAPA teaches the above deficiency of having a system wherein the register set is ACPI compliant **[see AAPA, Page 7, Paragraph 2 – Page 9, Paragraph 3]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of Luke with that of AAPA in order to take advantage of a more efficient power management interface with regards to the register set. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the teachings of Luke with that of AAPA in order to take advantage of a more efficient power management interface with regards to the register set.

16. **As per Claim 4, 13 and 22**, Luke as modified by AAPA above teaches SMBus message handler further comprising a buffer pointer register **[Fig. 6, element 92]** for pointing at one of a plurality of data registers **[Fig. 3, element 66]**; said finite state machine **[Fig. 6, element 82]** transferring data read from SMBus interface to the data register at which said buffer pointer register points if said finite-state machine interprets a "receive data to" instruction; said finite state machine transferring the data read from the data register at which said buffer pointer register points to **[Col. 7, Line 58-65]** said SMBus interface if said finite-state machine interprets a "transmits data from" instruction **[Col. 8, Line 66-Col.9, Line 4]**

17. **As per Claims 5, 14, 23 and 25** Luke as modified by AAPA above teaches SMBus message handler wherein the finite-state machine causes said buffer pointer register to be incremented each time a "transmit data to" or a "transmit data from" instruction is executed **[Col. 7, Lines 52-57]**

18. **As per Claims 24 and 27,** Luke as modified by AAPA above teaches a method wherein said transferring step further comprising decrementing a loop counter and checking as to whether said loop counter has a value of zero **[Col. 8, Lines 3-13]**.

19. **As per Claim 26,** Luke as modified by AAPA above teaches a method wherein said transferring step further comprising incrementing of said buffer pointer register **[Col. 7, Lines 44-50]**

(10) Response to Argument

20. Appellant argues that prior art of record fails to teach a "finite state machine configured to receive and interpret the instructions read by said instruction fetch unit..."

21. With respect to above argument, **Examiner disagrees**. Appellant argues that the combination of prior art, specifically Stancil and Luke, does not teach the above limitation because the finite state machine of Stancil is not coupled with a Instruction Fetch Unit (IFU) and thus would not be configured to receive and interpret instructions from said instruction fetch unit. However, to understand the Examiner's position, it must be noted that the difference between the Stancil reference and Luke et al is the fact that Luke is directed towards a Universal Serial Bus (USB) controller whereas Stancil discloses a SMBus controller comprising an SMBus interface, SMBus message handler and Finite-state machine configured to receive and interpret packets from the host. Furthermore, it should be noted that Stancil's state machine **(see Fig. 2, element 112 & 116)** receives instructions from host test system **(102)** and processes the instructions to create JTAG-compliant communication **(see Col. 4, Lines 14-32)**. Having established that Stancil's state machine is configured to retrieve and "interpret" (Note - Claims simply require the instructions to be received and interpreted and not necessary executed) instruction, it follows that the combination of Stancil with Luke allows the controller to retrieve the said instructions from a different source such as an Instruction Fetch Unit **[See Luke, Fig. 6 - element 82 (State Machine) & "Op Code Latch" (90)]** of Luke instead of host system of Stancil. Outside of addressing the limitation of a controller adapted to interface with SMBus specifically, it would be obvious to one of ordinary skill to include elements of a USB controller amongst Applicant's SMBus host controller. Therefore it is the position of the Examiner that the prior art fully reads on the claimed invention.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Jasjit S Vidwan/

Examiner, Art Unit 2182

Conferees:

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117

/Ilwoo Park/
Primary Examiner, Art Unit 2182